



LA Techniques Ltd

LA19-02-01 12 Gb/s PULSE PATTERN GENERATOR



The LA19-02-01 is a pseudo random pulse pattern generator capable of operation up to 12 Gb/s. The unit can accommodate two internal clock generators and it accepts an external clock input. It provides a fast pulse output up to 4 V_{pp} suitable for applications such as testing high bit rate communication components, fast pulse amplifiers and high speed logic circuit development.

- Operation to 12 Gb/s
- 35 ps rise and fall times
- Choice of pattern lengths
- User-programmable 128 bit pattern
- 4 V_{pp} adjustable output amplitude
- Low noise internal clocks
- Remote control through serial interface
- Low cost

Electrical Specification

Main and Auxiliary Outputs Signal Patterns

2²³-1 (conforms to CCITT) and 2⁷ (zero substitution) PRBS
 Clock/2, Clock/4, Burst and
 128 bit user-programmable

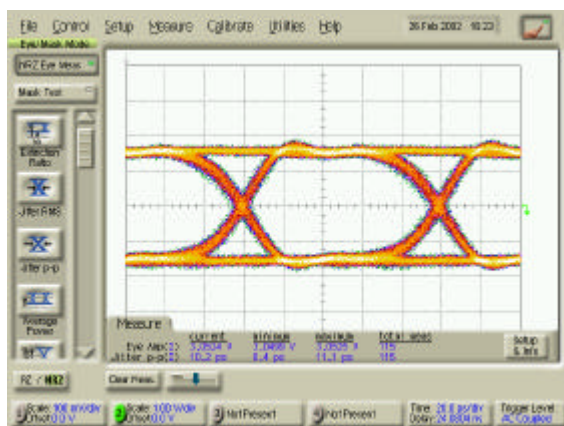
Parameter	Units	Min	Typ	Max
Operating Frequency				
Internal clock 1 (factory set) – Note 1	GHz	2.0	-	12.0
Internal clock 2 (factory set) – Note 1	GHz	2.0	-	12.0
External clock – Note 2	GHz	2.0	-	12.0
External clock input level				
12 GHz	dBm	9.0	10.0	13.0
10 GHz	dBm	6.0	10.0	13.0
2 GHz	dBm	4.0	6.0	13.0
Main Output (ac-coupled output) – Notes 3,4,5				
Output level (user adjustable)	V _{pp}	2.0	-	4.0
Setting resolution	V	-	-	0.1
Setting accuracy	%	-	5	-
Rise / fall time (10-90%)	ps	-	35	40
Jitter	ps (pp)	-	12	18
Crossover adjustment range (3V _{pp} output)	%	-	+/-5	-
Maximum Ratings				
dc offset (through internal bias-T)	V	-10	-	+15
Internal bias-T dc current	mA	-	-	100
Auxiliary Output – Notes 4,5				
(Main output with options 1 & 2) – Notes 4,5				
Output level (fixed)	V _{pp}	0.5	0.7	1.2
Jitter	ps (pp)	-	9	14
Synchronising Outputs Levels				
Clock	V _{pp}	0.4	0.7	2.0
Clock/16	V _{pp}	0.4	0.8	2.0
Pattern (not available on 2 ²³ -1 PRBS setting)	V _{pp}	0.4	0.8	2.0
Clock output phase adjustment range (12 GHz)	deg	450	540	-
Internal clocks stability	ppm/°C	-	0.3	1
SSB phase noise (12 GHz, 10 kHz offset)	dBc/Hz	-	-	-70
Maximum Ratings				
Clock Output dc offset (through internal bias-T)	V	-10	-	+15
Clock Output dc offset current	mA	-	-	100
Remote control serial interface data rate	bps	-	1200	-
Operating temperature range	°C	+15	-	+30
Power	Selectable ac 110-120 V (60Hz) and 220-245 V (50Hz), <100 W			
Dimensions (excluding carrying handle)	470 x 155 x 315 mm (W x H x D)			
Weight	<7 Kg			
Notes:				
1. Internal clock(s) are fixed frequency, user specified and set during manufacture				
2. Maximum external clock frequency typically up to 12.5 GHz				
3. Data output is non-inverted, non-return to zero (NRZ)				
4. Measured on 2 ²³ -1 PRBS setting, 10 Gb/s clock. Auxiliary output is the same polarity as main output				
5. Jitter measured on Agilent 86110A, synchronised to the clock and the reading taken after 100 measurements				

The LA19-02-01 provides a binary sequence signal synchronised to either an internal or external clock. The sequences available are pseudo random ($2^{23}-1$ and 2^7), clock/2, clock/4, burst and a user-programmed 128 bit sequence. The $2^{23}-1$ PRBS sequence is in accordance with the CCITT recommendation and the sequence is non-inverted. The 2^7 PRBS sequence is a zero substitution pattern where the longest run of zeros has been extended to eight zeros and the following bit set to one, thereby making the sequence 128 bits long.

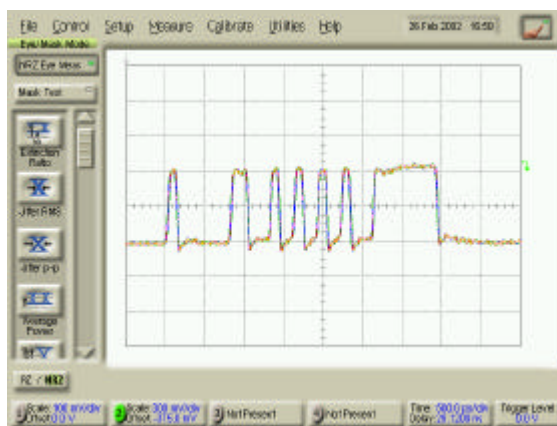
The main output is ac-coupled and provides a user adjustable 2 to 4 V_{pp} signal with fast transitions of 35 ps. An internal bias-T is provided to allow a dc offset to be superimposed on the main data output. The bias-T supports a dc current of up to 100 mA. The waveform crossover can be adjusted over a range of $\pm 5\%$ from the front panel. The auxiliary data output is a dc coupled, logic level output (0 to -0.8 V typical) with the same signal polarity as the main output.

Three types of synchronisation output signals are available, Clock, Clock/16, and Pattern. The clock is a sine wave with a typical amplitude of 0.8 V_{pp}. The clock/16 is derived from the clock signal by means of low noise dividers. The typical amplitude of this is 0.8 V_{pp}. The pattern synchronisation output produces an output synchronised to the length of the sequence selected. This allows, for example, the individual data bits to be observed on a sampling oscilloscope. It is available on all settings except the $2^{23}-1$ pattern length setting.

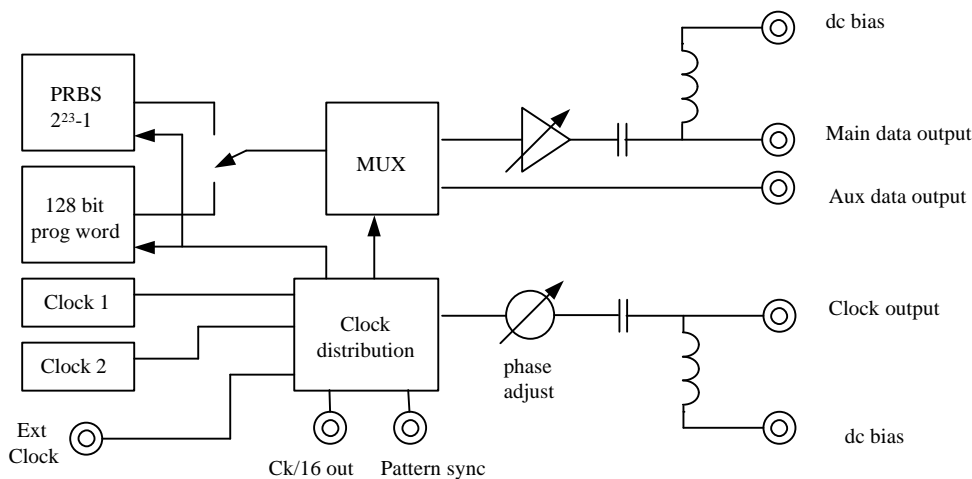
A bias-T is included on the clock output. This allows a dc offset to be added to the ac clock signal. The maximum dc current allowed is 100 mA. Also, the clock output includes a mechanically adjustable phase shifter able to provide at least 540° of phase shift at 12 GHz.



10 Gb/s, $2^{23}-1$ Pattern Eye Diagram



Example of user-programmable pattern



Simplified Block Diagram

Programmable Pattern

A 128 bit user-defined pattern can be programmed into the LA19-02-01 via the front panel. This is stored and retained indefinitely in internal memory until re-programmed. The auxiliary data output is dc-coupled and this will maintain waveform fidelity even when the programmed pattern entered is unbalanced.

Remote Control

An RS232 serial interface allows remote control of the instrument. This allows most front panel settings to be remotely adjusted. The exceptions are the clock phase shift and the main output crossover settings. The serial interface supports a single baud rate of 1200 bits per second.

Available Options

Option 1 removes the 4V output voltage capability and associated bias-T and substitutes it with a dc coupled, logic level (0.8 V, typical) low jitter output (Q). The auxiliary output then becomes an inverted data output (Q bar).

Option 2 provides the same logic level outputs as option 1 but with the Q output being ac coupled together with an internal bias-T to provide a dc offset.

ORDERING INFORMATION

LA19-02-01 Pattern generator

Clock1 xx GHz (xx is frequency in the range 2 to 12 GHz)

Options

Clock2 xx GHz (xx is frequency in the range 2 to 12 GHz)

Option 1: Removes 4 V ac coupled, adjustable output and substituted with a dc coupled, fixed level, low jitter output. This option provides dc coupled Q and Qbar outputs

Option 2: As option 1 but with the Q output ac coupled and including a bias-T to allow a dc offset to be superimposed on the data.



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